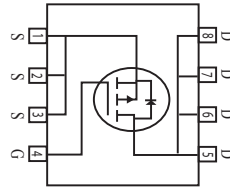


Surface Mount P-Channel Enhancement Mode MOSFET

(Pb) Lead(Pb)-Free



DRAIN CURRENT
-6 AMPERES
DRAIN SOURCE VOLTAGE
-30 VOLTAGE

Features:

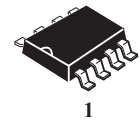
*Super high dense cell design for low $R_{DS(ON)}$

$R_{DS(ON)} < 35 \text{ m}\Omega @ V_{GS} = -10\text{V}$

$R_{DS(ON)} < 55 \text{ m}\Omega @ V_{GS} = -4.5\text{V}$

*Rugged and Reliable

*SO-8 Package



1
SO-8

Maximum Ratings (TA=25°C Unless Otherwise Specified)

Rating	Symbol	Value	Unite
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ($T_J = 125^\circ\text{C}$) ⁽¹⁾	I_D	-6	A
Pulsed Drain Current ⁽²⁾	I_{DM}	-30	A
Drain-Source Diode Forward Current (1)	I_S	-1.7	A
Power Dissipation (1)	P_D	2.5	W
Maximax Junction-to-Ambient	$R_{\theta JA}$	50	$^\circ\text{C/W}$
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

Device Marking

WT4433AM=STM4433A

Electrical Characteristics (T_A = 25 °C Unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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Static (2)

Drain-Source Breakdown Voltage V _{GS} =0V, I _D =-250 uA	V _{(BR)DSS}	-30	-	-	V
Gate-Source Threshold Voltage V _{DS} =V _{GS} , I _D =-250 uA	V _{GS(th)}	-1	-1.9	-3.0	V
Gate-Source Leakage Current V _{DS} =0V, V _{GS} =±20V	I _{GSS}	-	-	±100	nA
Zero Gate Voltage Drain Current V _{DS} =-24V, V _{GS} =0V	I _{DSS}	-	-	-1	uA
Drain-Source On-Resistance V _{GS} =-10V, I _D =-5.8A V _{GS} =-4.5V, I _D =-2.0A	R _{DS(on)}	- -	21 40	35 55	mΩ
On-State Drain Current V _{DS} =-5V, V _{GS} =-10V	I _{D(on)}	-20	-	-	A
Forward Transconductance V _{DS} =-15V, I _D =-5.8A	g _{fs}	-	8.5	-	S

Dynamic(3)

Input Capacitance V _{DS} =-15V, V _{GS} =0V, f=1MHZ	C _{iss}	-	920	-	PF
Output Capacitance V _{DS} =-15V, V _{GS} =0V, f=1MHZ	C _{oss}	-	270	-	
Reverse Transfer Capacitance V _{DS} =-15V, V _{GS} =0V, f=1MHZ	C _{rss}	-	170	-	

Switching (3)

Turn-On Delay Time V _D =-15V, V _{GEN} =-10V, I _D =-1A, R _{GEN} =6Ω	t _{d(on)}	-	8.6	-	nS
Rise Time V _D =-15V, V _{GEN} =-10V, I _D =-1A, R _{GEN} =6Ω	t _r	-	35.3	-	nS
Turn-Off Time V _D =-15V, V _{GEN} =-10V, I _D =-1A, R _{GEN} =6Ω	t _{d(off)}	-	36.9	-	nS
Fall Time V _D =-15V, V _{GEN} =-10V, I _D =-1A, R _{GEN} =6Ω	t _f	-	36.3	-	nS
Total Gate Charge V _{DS} =-15V, V _{GS} =-10V, I _D =-5.8A V _{DS} =-15V, V _{GS} =-4.5V, I _D =-5.8A	Q _g	- -	17.5 9.4	- -	nc
Gate-Source Charge V _{DS} =-15V, V _{GS} =-10V, I _D =-5.8A	Q _{gs}	-	2.9	-	nc
Gate-Drain Charge V _{DS} =-15V, V _{GS} =-10V, I _D =-5.8A	Q _{gd}	-	4.8	-	nc
Drain-Source Diode Forward Voltage V _{GS} =0V, I _S =-1.7A	V _{SD}	-	-0.77	-1.2	V

- Note: 1. Surface Mounted on FR4 Board t ≤ 10sec.
 2. Pulse Test : Pulse Width ≤ 300us, Duty Cycle ≤ 2%.
 3. Guaranteed by Design, not Subject to Production Testing.

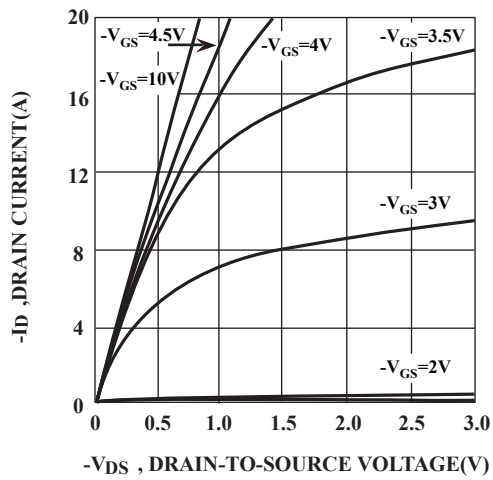


FIG.1. Output Characteristics

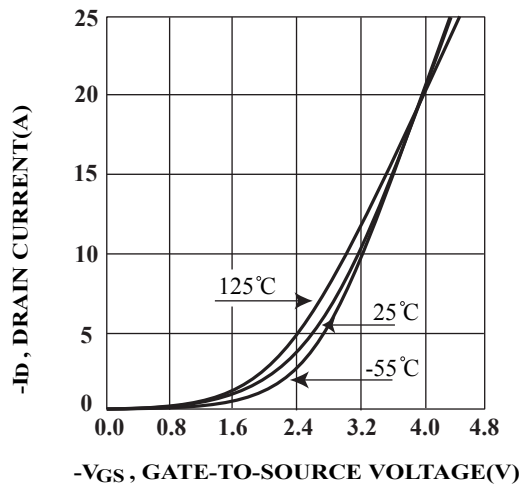


FIG.2 Transfer Characteristics

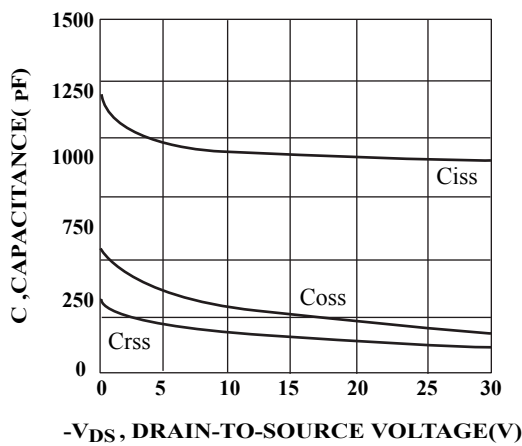


FIG.3 Capacitance

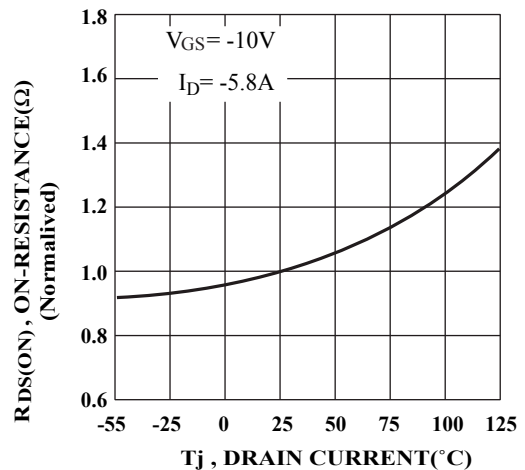


FIG.4 On-Resistance Variation with Temperature

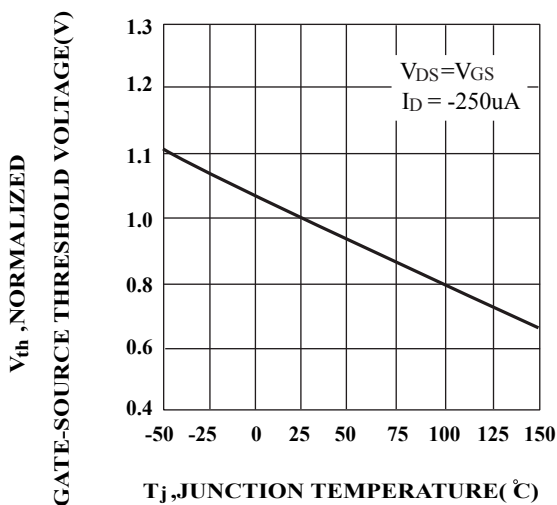


FIG.5 Gate Threshold Variation with Temperature

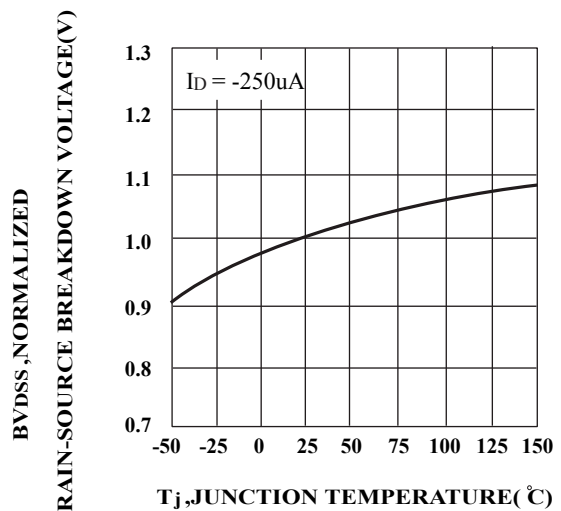


FIG.6 Breakdown Voltage Variation with Temperature

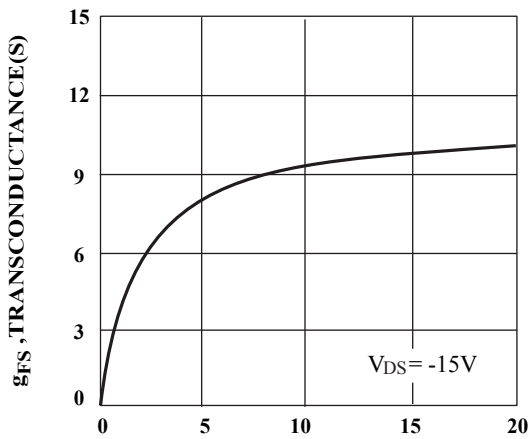


FIG.7 Transconductance Variation with Drain Current

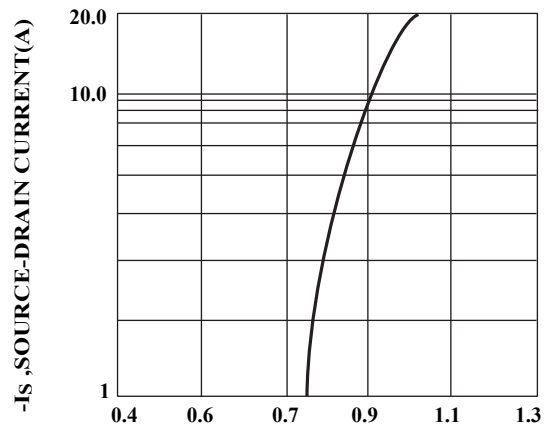


FIG.8 Body Diode Forward Voltage Variation with Source Current

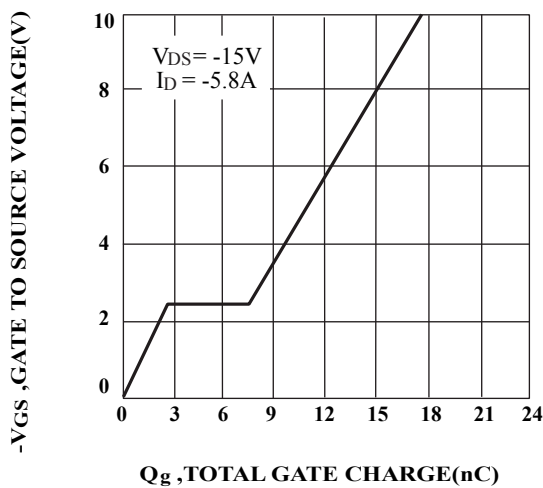


FIG.9 Gate Charge

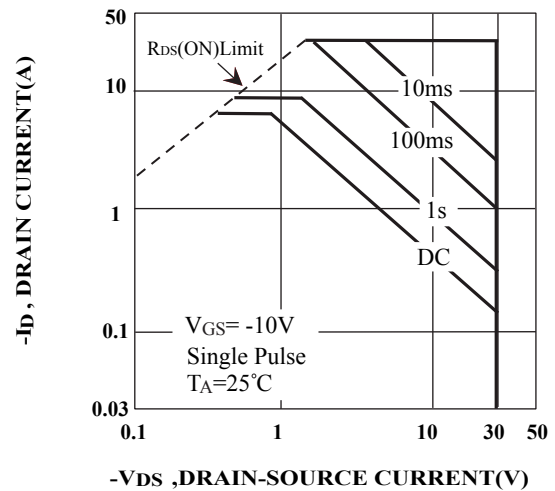


FIG.10 Maximum Safe Operating Area

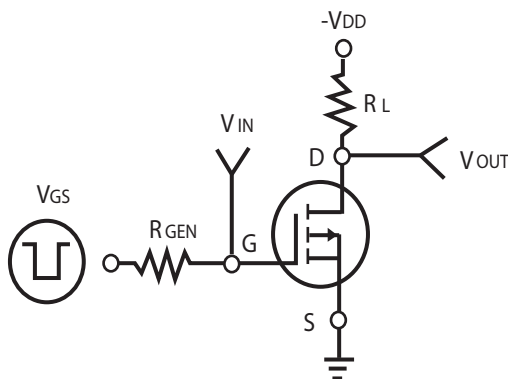


FIG.11 Switching Test Circuit

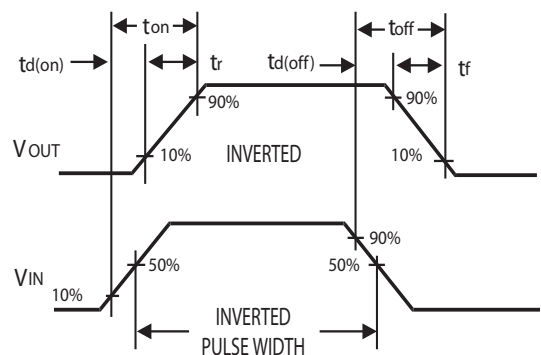


FIG.12 Switching Waveforms

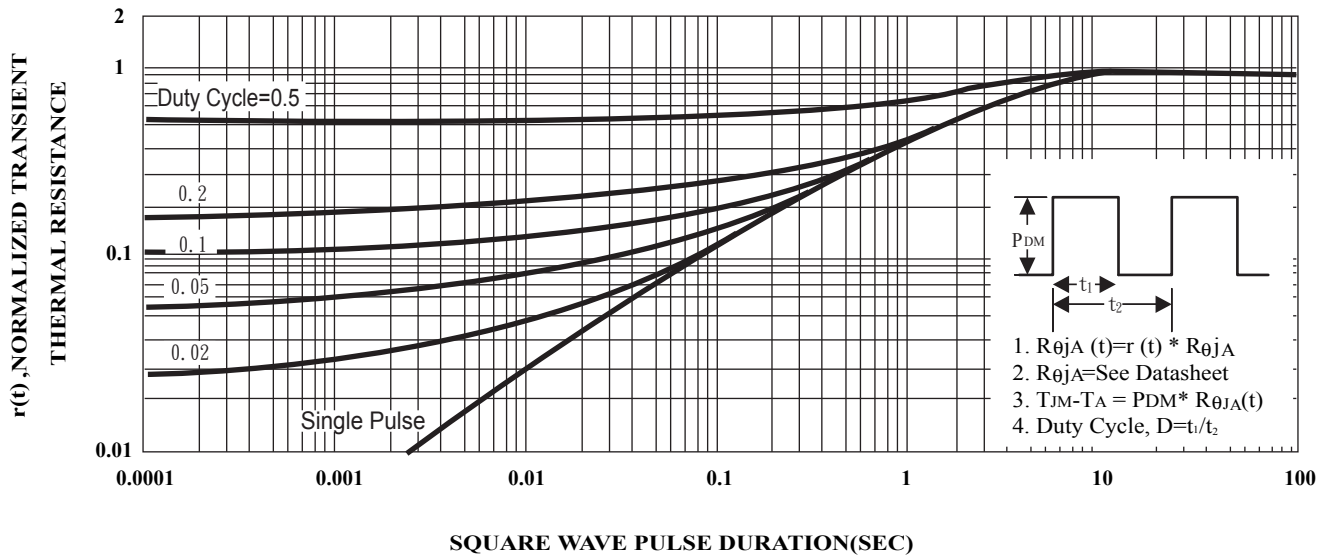
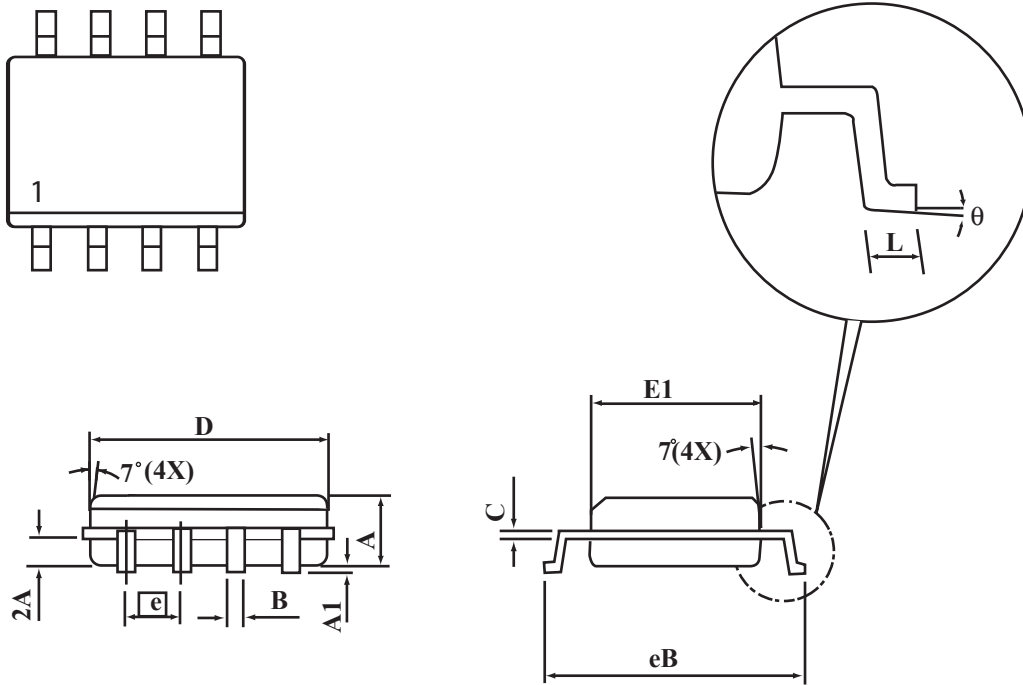


FIG.13 NORMALIZED THERMAL TRANSIENT IMPEDANCE CURVE

SO-8 Package Outline Dimensions

Unit:mm



SYMBOLS	MILLIMETERS	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.20
B	0.35	0.45
C	0.18	0.23
D	4.69	4.98
E1	3.56	4.06
eB	5.70	6.30
e	1.27 BSC	
L	0.60	0.80
θ	0°	8°